REMARKS

Summary of the Invention

Claims 78-108 of the present continuation application are directed to a method for fabricating a semiconductor component, such as a semiconductor package 130 (Figure 8). The method includes the step of providing a substrate 10 (Figure 1A) having a first side (face side 14-Figure 1A) and a second side (backside 16-Figure 1A). The method also includes the step of forming a plurality of openings 30 (Figure 1B) in the substrate 10, extending from the first side (face side 14-Figure 1A) to the second side (backside 16-Figure 1A). In addition, the method includes the step of forming conductive members 34 (Figure 1D) in the openings 30 by depositing a solder metal into the openings 30 using capillary action or a solder wave (page 12, lines 22-25 of the specification).

Drawings

The drawings have been objected to under 37 CFR 1.83(a) as not showing every feature of the invention specified in the claims. These objections are based on the drawings not showing the feature of "forming insulating layers in the opening" in claim 105, and the feature of "the conductive members comprise layers of solder on sidewalls of the opening" in claim 103.

These objections are traversed, as the drawings show both of these features. In this regard, the insulating layers 24A are shown in Figures 1C, 1D, 3A and 3. In addition, the step of "forming the insulating layers" is described on page 12, lines 10-19 of the specification.

Further, Figure 3B shows the conductive member 34A as being a layer on the sidewalls of the opening 30. As stated on page 18, lines 17-19 of the specification "the conductive members 34A comprises a conductive layer deposited on the sidewalls off the opening 30 rather than filling the entire opening 30".

Claim Rejection Under 35 USC §102

Claims 78-81, 90-95, 99-102 and 106-107 have been rejected under 35 USC 102(e) as being anticipated by Sarkhel et al. (US Patent No. 5,874,043) and Brusic et al. (US Patent No. 5,960,251), separately.

Claims 78, 81-84, 86-87, 90, 93, 97-99, 102 and 108 have been rejected under 35 USC 102(b) as being anticipated by Tanielian (US Patent No. 5,166,097).

Claims 78, 81, 85-90, 93-95, 99, 102, 104 and 106-107 have been rejected under 35 USC 102(b) as being anticipated by Leary-Renick (US Patent No. 4,622,058).

Claims 78, 81, 90, 93-96, 99, and 102-107 have been rejected under 35 USC 102(e) as being anticipated by Koh et al. (US Patent No. 5,599,744).

Claims 78-79, 81, 90, 92-95, 99, 101-102 and 106-107 have been rejected under 35 USC 102(b) as being anticipated by Bitaillou et al. (US Patent No. 4,830,264).

Claims 78, 81, 85-90, 93-95, 99, 102-104 and 106-107 have been rejected under 35 USC 102(b) as being anticipated by Lynch (US Patent No. 4,954,313).

Claims 78-81, 90-95, 99-102 and 106-107 have been rejected under 35 USC 102(e) as being anticipated by Brusic et al. (US Patent No. 5,960,251).

The following "Claim Chart" summarizes the rejections under 35 USC §102. In response to the rejections under 35 USC §102, the claims have been amended.

Claim Chart of 35 USC §102 Rejections

Claim	Sarkehl	Brusic	Tanielian	Leary-Renick	Koh	Bitaillou	Lynch	Brusic
78	X	X	X	X	X	X	X	X
79	X	X				X		X
80	X	X						X
81	X	X	X	X	X	X	X	X
82			X					
83			X					
84			X					
85				X			X	
86			X	X			X	
87			X	X			X	
88				X			X	
89				X			X	
90	X	X	X	X	X	X	X	
91	X	X						X
92	X	X				X		X
93	X	X	X	X	X	X	X	
94	X	X		X	X	X	X	
95	X	X		X	X	X	X	
96					X			
97			X					
98			X					
99	X	X	X	X	X	X	X	X
100	X	X						X
101	X	X				X		X
102	X	X	X	X	X	X	X	
103					X	X	X	
104				X	X	X		
105					X			
106	X	X		X	X	X	X	
107	X	X		X	X	X	X	
108			X					

Argument

Each independent claim (claims 78, 90 and 99) has been amended to recite the feature of the "substrate comprising a semiconductor material", and to recite the step of "forming the insulating layers in the openings". In addition, each independent claim (claims 78, 90 and 99) has been amended to recite that the substrate includes contacts (contacts 32-Figure 1D), and that the openings (openings 30-Figure 1B) are formed "through the contacts and the substrate" (see Figure 1B).

Antecedent basis for the "semiconductor material" recitation is contained on page 8, line 8 of the specification. Antecedent basis for the "forming the insulating layers" recitation is provided on page 12, lines 10-19 of the specification. Antecedent basis for the "through the contact" recitation is contained on page 11, lines 20-24 of the specification.

As none of the cited art anticipates these recitations in combination, the claimed method is submitted to be novel over the art. The claimed method is also submitted to be unobvious over the art. One indicia of unobviousness is that an improved component is provided, as the conductive members provide straight line electrical paths through the substrate from contacts on the substrate.

Rejected dependent claim 105 had recited the feature of the substrate comprising a semiconductor material, and the step of forming insulating layers 24A (Figure 1C) in the openings 30 prior to the forming the conductive members 34 (Figure 1D). As indicated by the "Claim Chart", claim 105 has only been rejected under 35 USC §102 over Koh et al. However, Koh et al. discloses a "method for forming conductive vias in a non-conductive substrate" (abstract). A non-conductive material is not the same as a semiconductor material as presently claimed. Further, with a non-conductive material an insulating step is not required. In this regard, a gold coat 16 is applied

directly to the substrate 10 within the via through-hole 12 (column 8, lines 1-2). The glass coat 18 in Koh et al. does not electrically insulate the gold coat 16 from the substrate 10. In addition, the plug 20, is stated to be epoxy (column 7, line 41, column 8, line 4) rather than solder as presently claimed.

Although Tanielian discloses conductive feedthroughs in a silicon wafer having dielectric layers 12 (Figure 1D), the step of "filling", "depositing" or "exposing" openings to solder for making the feedthroughs is not suggested. In addition, none of the remaining references disclose the features of a semiconductor material, forming the openings through contacts, an insulating step, and solder filling, deposition or exposure in combination.

Conclusion

In view of the amendments and arguments, favorable consideration and allowance of claims 78-108 is requested. In addition to the amendments to the claims, the "Cross Reference To Related Applications" has been amended to include patent numbers for the issued parent applications, and to cite related applications.

Also being submitted with this Amendment is an Information Disclosure Statement. Should any issues arise that will advance this case to allowance, the Examiner is asked to contact the undersigned by telephone.

DATED this 10th day of August, 2005.

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August 10, 2005
Date of Signature

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